I claim:

1. An apparatus, comprising:
a first register to store default configuration data;
a second register coupled to the first register to store active configuration data;
an input circuit coupled to the second register; and
control logic coupled to the first register, the second register, and the input circuit to load the second register with data selected from either the default configuration data from the first register or input data from the input circuit.

2. The apparatus of claim 1, further comprising:
reset logic coupled to the first register and the second register, the reset logic to select between loading the second register with the default configuration data and retaining a previous content of the second register in the second register.

3. The apparatus of claim 2, wherein the reset logic includes:
a first reset line to carry a first reset signal to load default data from the first register into the second register.

4. The apparatus of claim 3,wherein the first reset line is a power-up reset line.

5. The apparatus of claim 2, where the reset logic includes:
a programmable selection circuit to store a selection value; and

a second reset line coupled to the programmable selection circuit to carry a second reset signal;

wherein a value in the programmable selection circuit is to determine if the second reset signal causes the second register to be loaded with the default configuration data from the first register or causes the second register to retain its data.

6. The apparatus of claim 5, wherein the second reset line is a warm-start reset line.

7. The apparatus of claim 1, wherein the input circuit is to receive write data from a data bus, the write data comprising programmable configuration data.

8. The apparatus of claim 1, wherein the first register is a non-volatile register.

9. The apparatus of claim 1, wherein the second register is a volatile register.

10. The apparatus of claim 1, wherein the default configuration data defines a first memory configuration and the programmable configuration data defines a second memory configuration.

11. A system, comprising:

a processor;

a memory subsystem coupled to the processor and comprising flash memory, the flash memory including:

a first register to store default configuration data;

a second register coupled to the first register to store active configuration data;

an input circuit coupled to the second register; and

control logic coupled to the first register, the second register, and the input circuit to load the second register with data selected between the default configuration data from the first register and input data from the input circuit.

12. The system of claim 11, further comprising:

reset logic coupled to the first register and the second register, the reset logic to select between loading the second register with the default configuration data and retaining a previous content of the second register in the second register.

13. The system of claim 12, wherein the reset logic includes:

a first reset line to carry a first reset signal to load default data from the first register into the second register.

14. The system of claim 13,wherein the first reset line is a power-up reset line.

15. The system of claim 12, where the reset logic includes:

a programmable selection circuit to store a selection value; and

a second reset line coupled to the programmable selection circuit to carry a second reset signal;

wherein a value in the programmable selection circuit is to determine if the second reset signal causes the second register to be loaded with the default configuration data from the first register or causes the second register to retain its data.

16. The system of claim 15, wherein the second reset line is a warm-start reset line.

17. The system of claim 11, wherein the input circuit is to receive write data from a data bus, the write data comprising programmable configuration data.

18. The system of claim 11, wherein the first register is a non-volatile register.

19. The system of claim 11, wherein the second register is a volatile register.

20. The system of claim 11, wherein the default configuration data defines a first memory configuration and the programmable configuration data defines a second memory configuration.

21. A method, comprising:

providing, in a memory device, a first register containing default configuration data;

selecting active configuration data from between the default configuration data in the first register and input data from an input logic circuit;

writing the active configuration data into a second register; and

using the active configuration data in the second register to specify a configuration.

22. The method of claim 21, wherein providing the first register includes providing a non-volatile register.

23. The method of claim 21, wherein writing into the second register includes writing into a volatile register.

24. The method of claim 21, further comprising:

loading the default configuration data from the first register into the second register upon assertion of a first reset signal.

25. The method of claim 24, wherein assertion of a first reset signal includes assertion of a power-up reset signal.

26. The method of claim 21, further comprising:

selecting, upon assertion of a second reset signal, between retaining the active configuration data in the second register and loading the default configuration data from the first register into the second register.

27. The method of claim 26, wherein assertion of a second reset signal includes assertion of a warm-start reset signal.

28. The method of claim 21, wherein selecting active configuration data includes selecting programmable configuration data from the input logic circuit to define an operational configuration of a memory that is different than defined by the default configuration data.

29. The method of claim 21, wherein selecting active configuration data includes selecting default configuration data to define a predetermined intended operational configuration of a memory.